IN THE CLAIMS

The current claims for this application are listed below:

1. - 4. (Canceled)

5. (Currently Amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated in response to changes in nominal system frequency while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable;

wherein a position of the profile in the profile memory, read by the profile state machine in sequence to control the PLL, is adjustable; and

~~The clock circuit of claim 4,~~ wherein the profile memory further stores address information about the profile, the address information specifying the number of entries of the profile and the position of the profile in the profile memory.

6. (Currently Amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated in response to changes in nominal system frequency while the PLL generating the clock signal;

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory; and

~~The clock circuit of claim 4, further comprising:~~

at least one register to store address information about the profile, the address information specifying the number of entries of the profile and the position of the profile in the profile memory;

wherein a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable; and

wherein a position of the profile in the profile memory, read by the profile state machine in sequence to control the PLL, is adjustable.

7. - 8. (Canceled)

9. (Currently Amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated in response to changes in nominal system frequency while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory

and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable;

wherein the profile memory is capable of simultaneously storing a plurality of profiles; and, the profile state machine is capable of being instructed to use one of the plurality of profiles to control the PLL; and

~~The clock circuit of claim 7,~~ wherein the plurality of profiles comprise one profile for slewing the clock signal from a first nominal clock frequency to a second nominal clock frequency.

10. (Original) The clock circuit of claim 9, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency in managing at least one of:

a) power consumption; and

b) thermal status;

of the data processing system.

11. (Original) The clock circuit of claim 9, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency in balancing power consumption and computational load of the data processing system.

12. - 16. (Canceled)

17. (Currently Amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein the profile memory is capable of simultaneously storing a plurality of profiles;

wherein the profile state machine is capable of being dynamically instructed to use one of the plurality of profiles to control the PLL in response to changes in nominal clock frequency; and

~~The clock circuit of claim 12,~~ wherein the clock circuit is capable of slewing the clock signal from a first nominal frequency to a second nominal frequency; and, the profile state machine is dynamically instructed to use one of the plurality of profiles for one of the first and second nominal frequencies.

18. (Original) The clock circuit of claim 17, wherein the clock signal is slewed to manage power and thermal status of the data process system.

19. (Currently Amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein the profile memory is capable of simultaneously storing a plurality of profiles;

wherein the profile state machine is capable of being dynamically instructed to use one of the plurality of profiles to control the PLL in response to changes in nominal clock frequency; and

~~The clock circuit of claim 12,~~ wherein the plurality of profiles comprise a first profile for spread spectrum modulating the clock signal of a first nominal frequency; the plurality of profiles comprise a second profile for spread spectrum modulating the clock signal of a second nominal frequency; and the plurality of profiles comprise a third profile for slewing the clock signal between the first and second nominal frequencies.

20. - 35. (Canceled)

36. (Currently Amended) A machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency;

~~The method of claim 35, further comprising:~~

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile, the second profile and a third profile;

spread spectrum modulating the clock signal at a first nominal frequency using the first profile;

slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile; and

spread spectrum modulating the clock signal at the second nominal frequency using the third profile;

wherein the profile memory is capable of being updated while the PLL generating the clock signal.

37. - 42. (Canceled)

43. (Currently Amended) A machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency; and

slewing the clock frequency from a first nominal frequency to a second nominal frequency;

wherein the profile memory is capable of being updated while the PLL generating the clock signal;

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency; and

~~The method of claim 41,~~ wherein the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

44. - 47. (Canceled)

48. (Currently Amended) A machine readable medium containing executable computer program instructions which when executed by a data processing system

cause said system to perform a method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency;

~~The medium of claim 47, wherein the method further comprises:~~

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile, the second profile and a third profile;

spread spectrum modulating the clock signal at a first nominal frequency using the first profile;

slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile; and

spread spectrum modulating the clock signal at the second nominal frequency using the third profile;

wherein the profile memory is capable of being updated while the PLL generating the clock signal.

49. - 54. (Canceled)

55. (Currently Amended) A machine readable medium containing executable computer program instructions which when executed by a data processing system cause said system to perform a method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency; and

slewing the clock frequency from a first nominal frequency to a second nominal frequency;

wherein the profile memory is capable of being updated while the PLL generating the clock signal;

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency; and

~~The medium of claim 53,~~ wherein the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

56. - 88. (Canceled)